ARM® Cortex™-M0

Smallest, Lowest Power ARM Processor Ever

The ARM® Cortex™-M0 processor is the smallest and lowest power 32-bit ARM processor available. The exceptional low power, small gate count and code footprint of the processor makes it ideal for ultra low power MCU and mixed signal applications, delivering 32-bit performance and efficiency in a 16-bit footprint.

The processor has been developed to address the need for performance efficiency, delivering 0.9 DMIPS/MHz in ultra low-cost MCUs and analog mixed signal and SoC applications, while retaining tool and binary compatibility with the feature-rich Cortex-M3 processor.

The Cortex-M0 processor, which consumes as little as 85 microwatts/MHz (0.085 milliwatts) in an area of under 12K gates when implemented using ARM Physical IP on a 180 ultra low leakage (ULL) process, builds on the unrivalled expertise of ARM as a leader in low-power technology and a key enabler for the creation of ultra low-power devices.

32-bit Performance and Efficiency

The demand for ever lower-cost portable products with increasing connectivity such as USB, GPS, Bluetooth, ZigBee, and novel interfaces, including accelerometers and touch screens, has resulted in the need to more tightly integrate analog devices with digital functionality to pre-process and communicate data.

The 32-bit Cortex-M0 processor's low cost and low power credentials, combined with ARM Thumb® technology for maximum code density, make it a perfect solution for these tasks.

ARM®
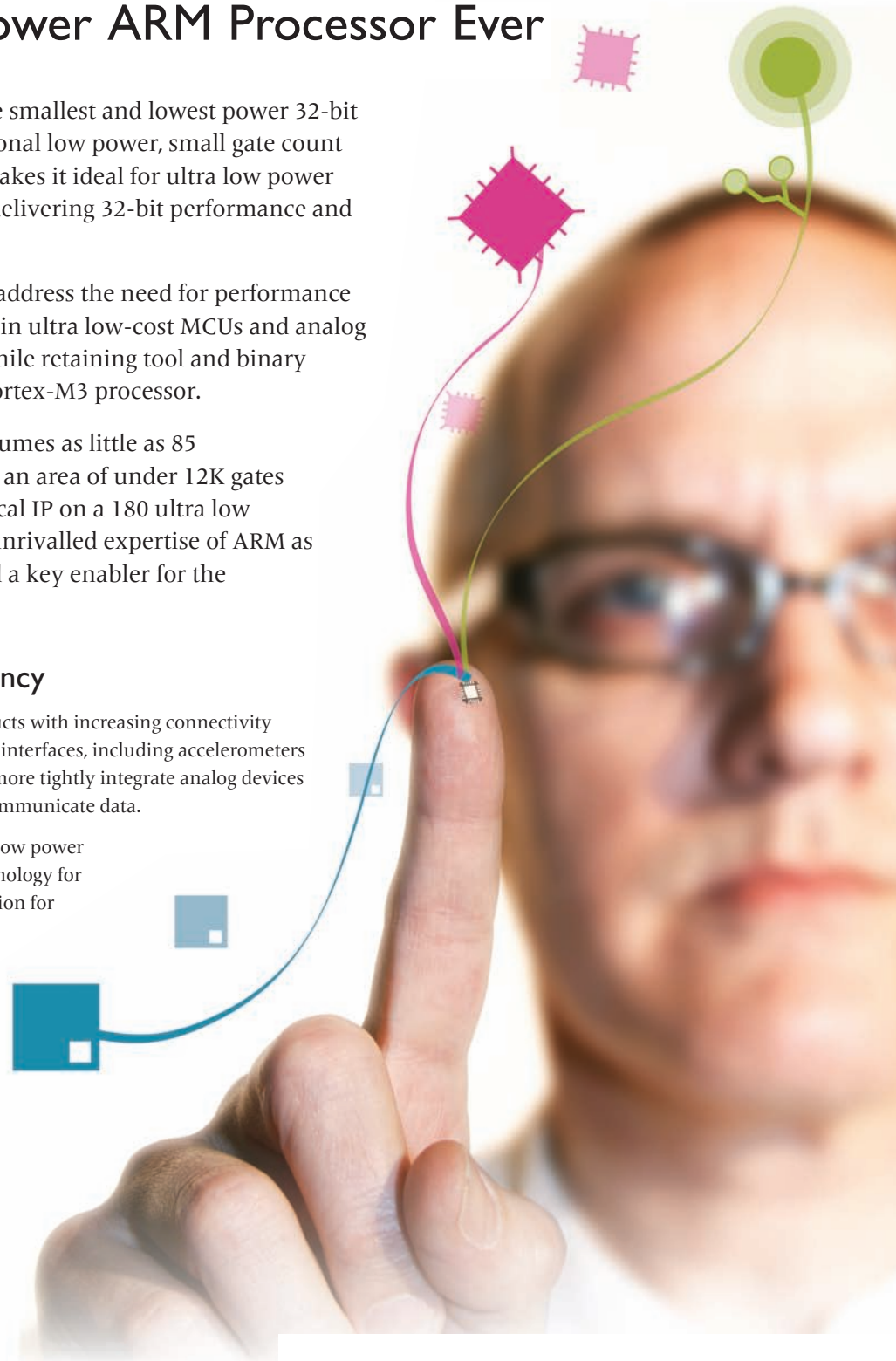
Key Benefits

The ARM Cortex-M0 processor offers significant benefits to system and software developers.

- 32-bit performance in a 16-bit footprint
- Power efficiency and longer battery life
- Performance headroom for product enhancements
- Small size enables the processor and analog circuits to be implemented on single die
- Lower cost devices through a smaller processing core, system and memories
- Ultra low power consumption and integrated sleep modes resulting in longer battery life

- Thumb® instruction set for maximum code density and minimum memory footprint
- Fast interrupt handling for critical control applications
- Wake-up Interrupt Controller enables ultra low leakage retention mode with instantaneous fully active mode for critical events
- Enhanced system debug for faster development
- 100 per cent C coding possible
- Wide application envelope encompassing ultra low cost microcontrollers and analog mixed signal applications
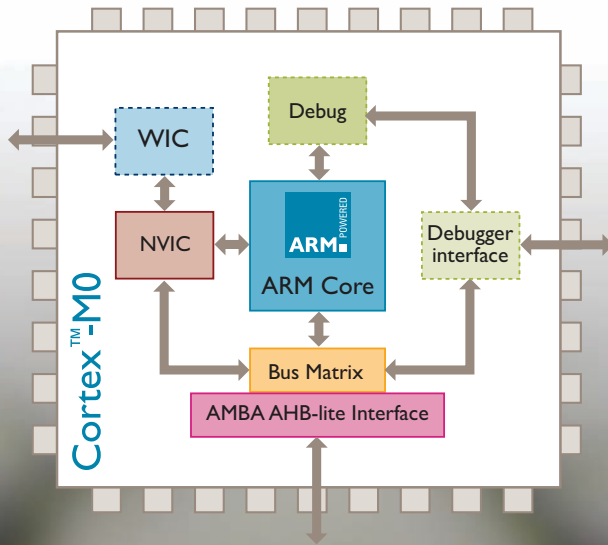
Applications

The new processor further extends the ARM Cortex-M processor roadmap into ultra low-power MCU and SoC applications, including:

- Medical devices
- e-metering
- Lighting
- Smart control
- Precision analog and mixed signal
- Gaming accessories
- Power supply control
- Motor control
- IEEE 802.15.4 (ZigBee) and Z-Wave systems

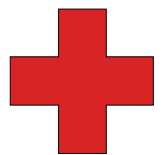Touchscreen, touchpad and accellorometer pre-processing

The Cortex-M0 processor is also suitable for programmable mixed signal applications such as intelligent sensors and actuators which have traditionally required separate analog and digital devices.
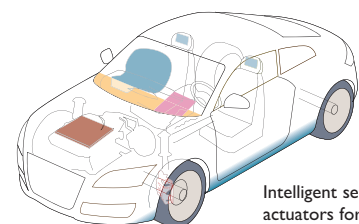

BLDC Motor control for white goods and industrial

Wireless (IEEE 802.15), USB and Ethernet connectivity

Ultra low power medical devices

Intelligent sensors and actuators for automotive

Cortex™-M0

WIC

Debug

NVIC

ARM POWERED

ARM Core

Debugger interface

Bus Matrix

AMBA AHB-lite Interface

Ultra Low Power

The Cortex-M0 processor is designed for extremely low dynamic power and leakage. Like all Cortex-M profile processors the Cortex-M0 processor also supports ultra low-power sleep implementation with the ARM 180ULL Power Management Kit (PMK) and standard cell libraries. Combined with the integrated Wake-up Interrupt Controller (WIC) this enables the core to be rapidly placed in an ultra low leakage state retention mode, returning to fully active mode almost instantaneously on critical events.

The Cortex-M0 processor also features a Nested Vectored Interrupt Controller (NVIC) closely coupled to the core. The Cortex-M0 NVIC supports 1 to 32 interrupts, multiple levels of interrupt priorities, and offers a rapid interrupt response that further enhances the responsiveness and energy efficiency of the processor.

The convergence of these technologies results in an extremely low power 32-bit processor that has the performance efficiency and responsiveness to minimize activity periods, and when implemented with ARM physical IP can achieve even lower power consumption in active and sleep states.
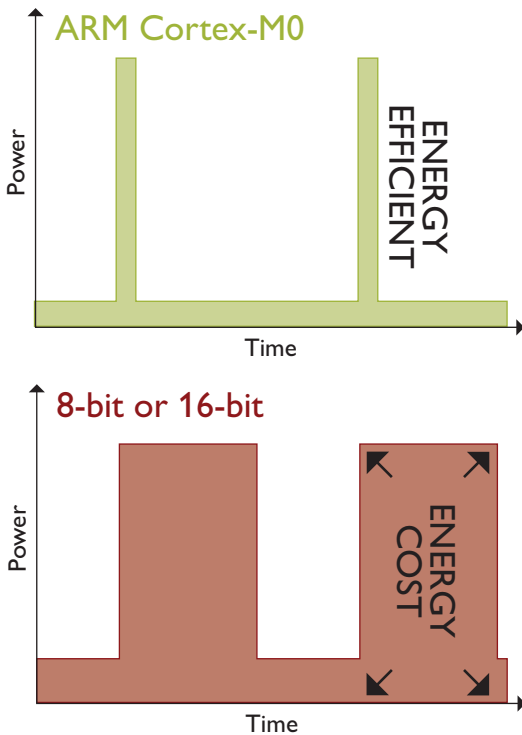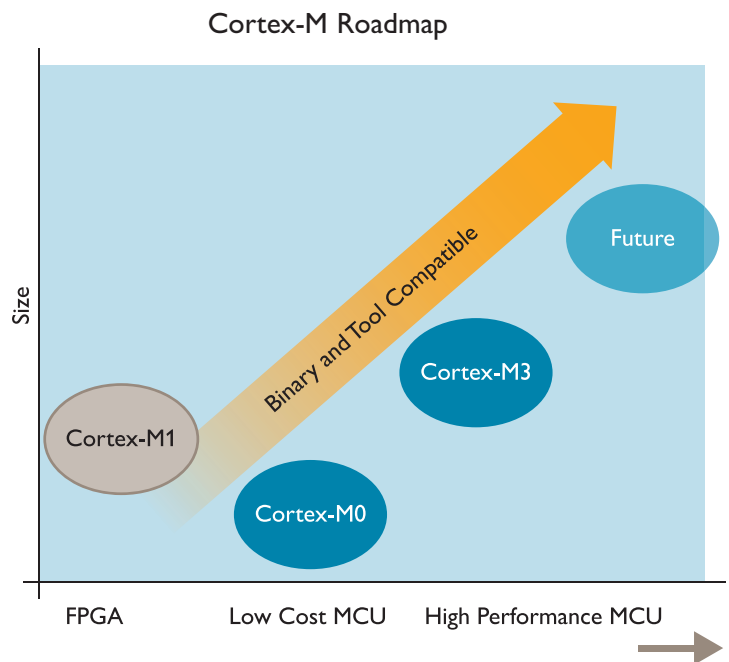
Simplicity and Compatability

The ARM Cortex-M0 processor implements a small instruction set architecture (ISA) consisting of just 58 fundamental instructions. This simple ISA is a superset of the 16-bit Thumb® ISA first implemented in the ARM7TDMI® processor, and has subsequently underpinned the ISA of every ARM processor developed since. The reason for the enduring popularity Thumb lies in its code density – this is crucial in embedded devices where the memory footprint can be the most significant proportion of the silicon cost.

The Cortex-M0 processor also incorporates many of the enhancements introduced in the ARM Cortex-M3 processor that enable further area savings and ensure upwards compatibility. Important examples of this are support for Thumb-2 and Thumb state exception handling, and the inclusion of the tightly integrated Nested Vectored Interrupt Controller (NVIC) that enables both Cortex-M0 and Cortex-M3 processorto achieve a low latency, deterministic interrupt response. The NVIC architecture, which automatically performs hardware stacking of corruptible registers on interrupt entry, removes the need for shadow registers within the processor. Correspondingly several Thumb-2 system instructions are included in the Cortex- M0 ISA to support this model and to ensure full upwards binary compatibility with Cortex-M3. To the embedded designer this translates to the benefits of a low processor gate count with a correspondingly low memory footprint requirement for software.

180ULL	65LP
Application – Low cost MCU, Mixed-signal devices	Application – System-on-Chip
DMIPS/MHz 0.90	DMIPS/MHz 0.90
Frequency 50MHz	Frequency 270MHz
Power: 0.085 mW/MHz	Power: 0.012 mW/MHz
Power efficiency: 10 DMIPS/mW	Power efficiency: 75 DMIPS/mW
Power and area estimates based of floorplanned trials of prototype	

ARM Cortex-M0

ENERGY EFFICIENT

8-bit or 16-bit

ENERGY COST

Cortex-M Roadmap

Binary and Tool Compatible

Future

Cortex-M3

Cortex-M1

Cortex-M0

Size

FPGA   Low Cost MCU   High Performance MCU

Tools Support

The Cortex-M0 processor is fully supported by the Keil™ Microcontroller Development Kit, which integrates the ARM

RealView® Compilation Tools with the Keil μVision4 IDE and Debugger.

The Keil μVision4 IDE has been designed to enhance developer's productivity, enabling faster, more efficient program development.

The Keil μVision4 introduces a flexible window management system, enabling you to drag and drop individual windows anywhere on

the visual surface including support for multiple monitors.

Keil μVision4 builds on the popular μVision3 IDE with the addition of:

- Multiple monitor support and flexible window management system
- System Viewer Windows - displays device peripheral register information
- Debug Restore Views - enables multiple debug window layouts to be created and saved
- Multi-project Workspace - simplifies working with numerous concurrent projects
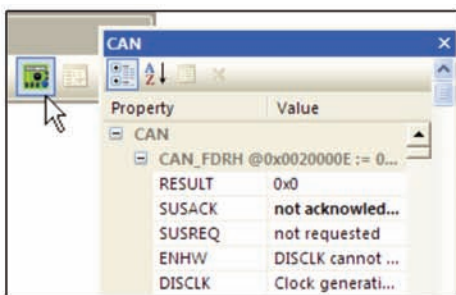
Physical IP

The low-power operation of the Cortex-M0 processor is enhanced by the ARM Ultra High Density Standard Cell Library and ARM Power Management Kit (PMK) for a 180ULL process, low power memory instances built specially for Cortex-M0, and the Keil™ Microcontroller Development Kit. The ARM low power libraries are optimized to enable low dynamic and static power consumption and minimize chip area. The PMK features dynamic and leakage power management functions and the low power memory instances support external power gating for extreme leakage reduction.

Software Standard

The Cortex-M0 processor is fully compatible with the recently-launched Cortex Microcontroller Software Interface Standard (CMSIS), the vendor-independent hardware abstraction layer for the Cortex-M processor series. The CMSIS enables consistent and simple software interfaces to the processor for silicon vendors and middleware providers, simplifying software re-use, reducing the learning curve for new microcontroller developers and reducing the time-to-market for new devices.

 The CMSIS is available for free download from www.onARM.com, a website providing a comprehensive resource for embedded developers. CMSIS documentation and maintenance of the software layer will be provided by ARM.

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Web:

www.arm.com/products/CPUs/ARM-Cortex-M0.html

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